6.4 A 1.1V 3.1-to-9.5GHz MB-OFDM UWB Transceiver in 90nm CMOS

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While extensive development of multi-band OFDM (MB-OFDM) UWB transceivers operating over the 3.1 to 4.8GHz band has taken place, the demand for those operating in higher bands is increasing because they could alleviate interference problems. This paper presents 1) a wideband frequency synthesis technique and 2) a parasitic-capacitance reduction technique that make wideband TX/RX possible, as well as 3) a pseudo-differential (PD) OTA with a high CMRR for achieving low supply voltage operations, and 4) a back-bias calibration mixer for attaining LO leakage suppression without degrading wideband RF characteristics. These proposed techniques make possible 3.1-to-9.5GHz MB-OFDM UWB transceivers in 90nm CMOS with 1.1V supplies.

Our transceiver has a direct-conversion architecture containing a frequency synthesizer that generates 12 bands over 3.1 to 9.5GHz, as shown in Fig. 6.4.1. The synthesizer consists of a single 8.4GHz quadrature-VCO (Q-VCO) and divide-by-two dividers, low frequency (LF) SSB mixers with a VGA for wideband LO power flatness, and high-frequency (HF) SSB mixers. All the LO frequencies needed for 3.1 to 9.5GHz operation are generated from this single Q-VCO, which contributes to low power consumption. The VCO frequency is low enough to use low-power D-latch-based frequency dividers. Both the Q-VCO and the dividers operate over a full voltage swing, which also contributes to high SNR even with low supply voltages. A harmonic suppressing filter is introduced at the LF mixer output terminal. The cut-off frequency of the filter is programmed to be switched in accordance with changing bands. Further, in order to maintain constant LF output power over a wide frequency range (from 792 to 1848MHz), the VGA that follows this filter is also programmed to change its gain, so that the LF output power is held constant. The configuration here results in a low measured power dissipation of 47mW, even for 3.1 to 9.5GHz synthesis.

Figure 6.4.2 is an LNA schematic. The LNA consists of a three-stage amplifier with a transistor ($M2$) in a deep N-well, as well as a shielded capacitor ($C1$). The source terminal of $M2$ is connected to the bulk terminal and to the shield plate of $C1$. Since the $M2$ source drives the drain-bulk capacitor, C_{db}, the influence of C_{db} decreases as a result of the Miller effect [1]. Moreover, our shielded $C1$ design achieves high-frequency characteristics because of its low $C1$-shield capacitance, also by means of the Miller effect. A conventional capacitor has a large substrate capacitance, and we could not use one for our dc-blocking capacitor. The use of these two techniques increases the cut-off frequency at the drain of $M2$ by about 1GHz. The voltage gain of the first stage is about 15dB. Each of the subsequent 2-stage amplifiers has a gain of about 6dB under the gain-bandwidth constraint, and thus the total gain achieved with this LNA is about 27 dB.

An RX LPF, shown in Fig. 6.4.1, requires especially high linearity in its RX paths, and needs to operate at a low supply voltage. This means the number of stacked transistors should be decreased. A PD OTA has been proposed to accomplish this [2], but it has a large common-mode voltage gain (see Fig. 6.4.3), $\approx g_{m1}/g_{m2}$, to its output signal current $I_+ - I_{CM}^*$. This gain is caused by an error in the mirrored common-mode current I_{CM}^* resulting from channel-length modulation. The common-mode gain induces severe common-mode problems in an RX LPF, which result from even-order distortion and/or substrate noise. In order to solve these problems, we have developed an error-rejecting technique for the PD OTA. In our OTA, an opposite phase signal $I_- - I_{CM}^*$ having nearly the same error is generated, and then subtracted from the output, $(I_+ - I_{CM}^*) - (I_- - I_{CM}^*)^*$. This eliminates almost all of the error, and the common-mode voltage gain is minimized to $\approx(g_{o1} + g_{o2})g_{m1}/g_{m2}/g_{m3}$. Simulations show the common-mode gain in this OTA to be about -30dB less than that in a conventional one. We have measured the differential and common-mode gains of our LPF, whose configuration is 3rd + 3rd-elliptic *gm-C*, and found CMRR to reach 48dB at 1MHz (Fig. 6.4.4). The common-mode gain is maintained below -20dB up to gigahertz levels, a level of wideband suppression that has not been obtained with conventional architectures [2].

Mixers operating in the gigahertz range with narrow-channel differential pairs have a serious problem of high LO leakage resulting from process variations. However, mixer-calibration in an UWB transceiver is difficult because the transceiver contains many mixers (e.g., Fig. 6.4.1's transceiver has two I/Q up-conversion mixers and four mixers in the HF SSB mixer block). For our mixers, we use a back-bias calibration design in which each mixer receives a calibration voltage from an analog bus [3] as shown in Fig. 6.4.5. A multi-level voltage generator (MLVG) generates five levels of coarse and four levels of fine correction voltages. These are distributed to individual mixers by way of the analog bus. Each mixer contains two MUXs; one MUX sends a coarse correction voltage to one of the back gates in the two differential pairs, and the other MUX sends a fine voltage to the other back gate. By choosing from among the 20 possible combinations (5 coarse and 4 fine) for each I and Q up-converter, it has been possible to decrease LO leakage to -36dBc. In this correction scheme, the only steady current is the 0.1mA at the MLVG. Note that this scheme supplies the correction signal to the back gate; no circuit is required to combine the correction signal with a baseband signal. This is important because such circuits often increase parasitic capacitance, thus degrading RF characteristics.

Figure 6.4.6 gives a performance summary. The transceiver was fabricated in an ASPLA 90nm 1P6M CMOS process without any additional thick metal. Phase noise at the TX output is -108 to -98dBc/Hz at a 1MHz offset from carriers across the 12 bands. Overall TX OIP3 and overall RX maximum gain are nearly flat up to 9.5GHz, and they exceed, respectively, 7.2dBm and 58dB. Overall NF is 6.3 to 7.8dB. IIP3 exceeds -17dBm at minimum gain across the 12 bands. The active area, excluding pads, is 3.5mm^2 (see Figure 6.4.7). Operating from a 1.1V supply, the transceiver dissipates 131mW in the TX mode and 224mW in the RX mode.

References:

[1] A. Bevilacqua and A. Niknejad, "An Ultrawideband CMOS Low-Noise Amplifier for 3.1-10.6-GHz Wireless Receivers," *IEEE J. Solid-State Circuits*, Vol. 39, No.12, pp. 2259-2268, Dec., 2004.

[2] A. Mohieldin et al., "Nonlinear Effects in Pseudo Differential OTAs with CMFB," *IEEE T. Circuits and Systems II*, Vol. 50, No.10, pp.762-770, Oct., 2003.

[3] A. Tanaka et al., "A Non-Uniformity Correction Scheme using Multiple Analog Buses for an Uncooled Infrared Sensor," *Symp. VLSI Circuits*, pp. 161-164, June, 2003.

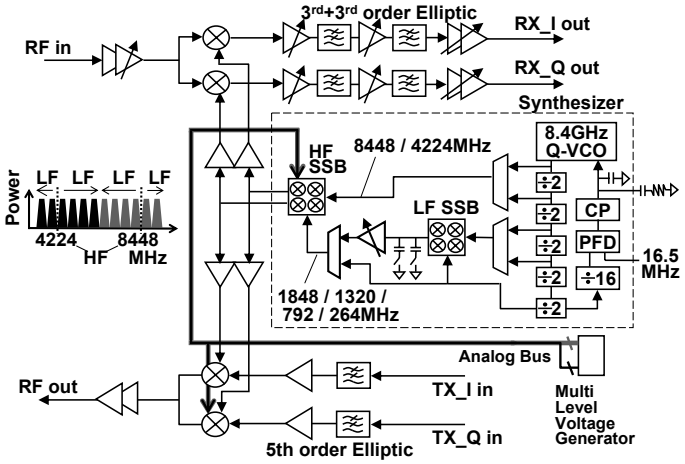

Figure 6.4.1: 3.1 to 9.5GHz UWB transceiver.

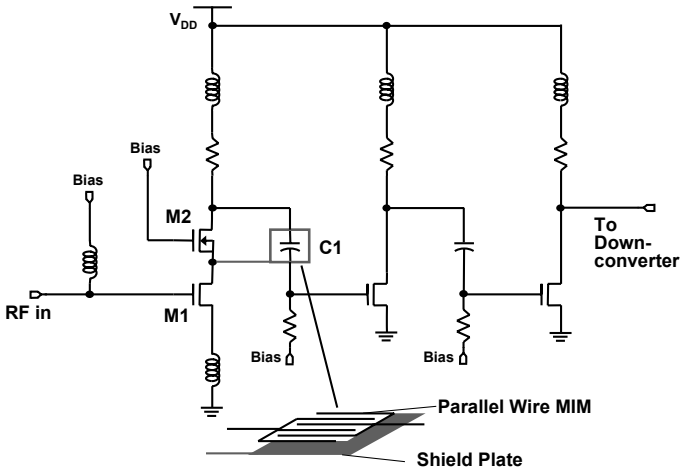

Figure 6.4.2: LNA schematic.

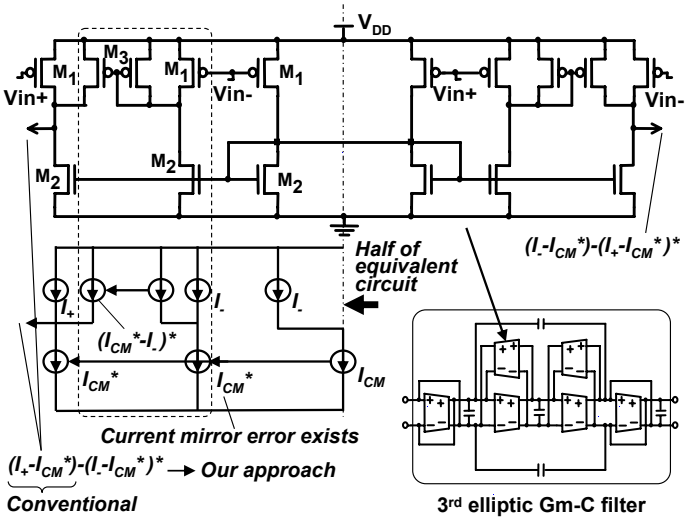

Figure 6.4.3: Common-mode rejection pseudo-differential OTA.

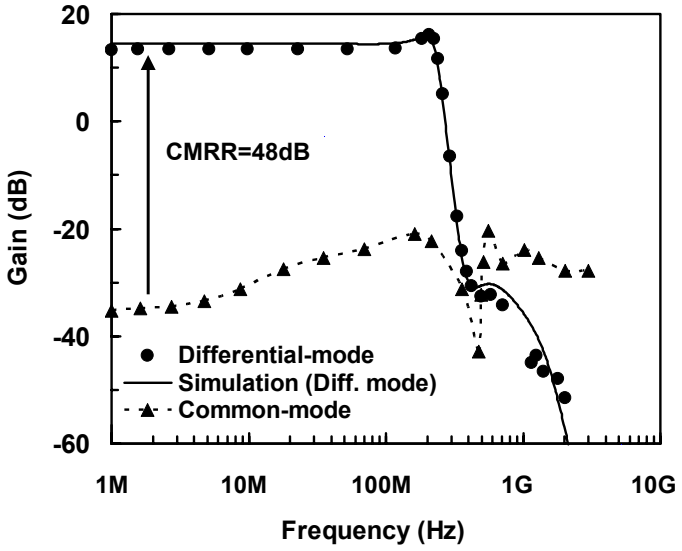

Figure 6.4.4: Measured LPF gain.

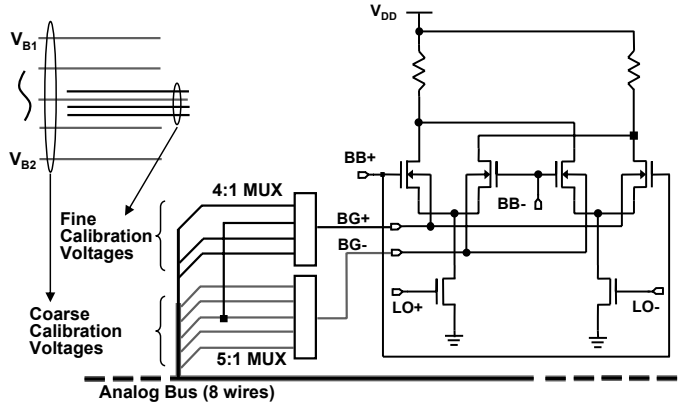

Figure 6.4.5: Analog bus bulk biasing.

Band Group	1	2	3	4
Band ID	1	5	8	12
Center frequency (MHz)	3442	5544	7128	9240
RX maximum gain (dB)	64.0	63.2	61.3	58.7
RX minimum gain (dB)	14.4	14.1	15.0	11.5
RX overall NF (dB)	6.9	6.3	6.5	7.8
RX in-band IIP3 (dBm) *	-16.5	-17.0	-16.0	-13.3
TX OIP3 (dBm)	8.6	8.3	8.6	7.2
Phase noise @1MHz (dBc/Hz)	-108	-103	-101	-98
Spurious tones (dBc)	-26	-23	-24	-20
LPF pass band frequency	2 ~ 233 MHz			
VCO frequency	8448 MHz			
Supply voltage	1.1 V			
TX power dissipation	131 mW			
RX power dissipation	224 mW			
Technology	90nm 1P6M CMOS			
Active area exclude pads	3.5 mm^2			

* In-band IIP3 are measured in minimum gain.

Figure 6.4.6: Performance summary.

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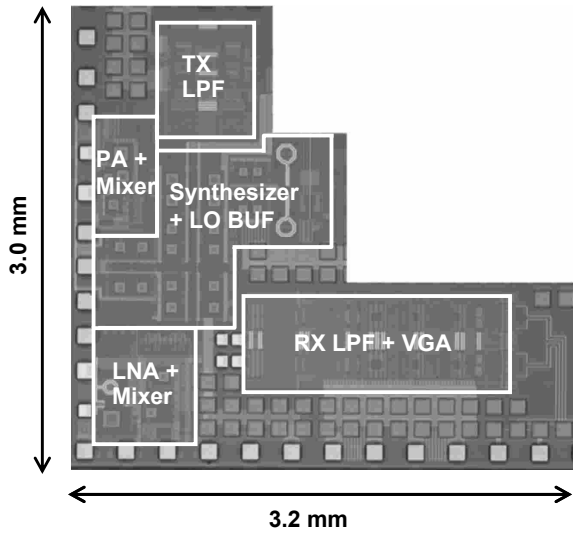

Figure 6.4.7: Micrograph of transceiver chip.

